

JUANG, TZUNG-HAN

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AREA OF INTEREST

Code Generation, Hardware Design, Machine Learning

EDUCATION

Mcgill University, QC, Canada	Current
PhD Student, Department of Electrical and Computer Engineering	
Northwestern University, IL, U.S.A.	Jun. 2020
Master's Degree, Department of Computer Science	
National Taiwan University (NTU), Taiwan	Jun. 2018
Master's Degree, Graduate Institute of Electronics Engineering	
National Cheng Kung University (NCKU), Taiwan	Jun. 2016
Bachelor's Degree, Department of Electrical Engineering	

WORK EXPERIENCE

Assembly/Test Technology Development (Internship), Intel	Jun. 2020 – Sep. 2020
- Optimize code and apply machine learning to a part of the solver for production line management	
Agile Manufacturing System for Intel production line (Research Assistant for Prof. Klabjan)	Jun. 2019 – Jun. 2020
- Use reinforcement learning to manage a production line in Intel	
- Design simulation environment to model a real-world production line	
System Administrator for Magics Lab	Mar. 2019 – Dec. 2019
- Manage a Kubernetes cluster	
Teaching Assistant for the course IC design (3 semesters), NTU	Mar. 2017 – Jul. 2018
- Teach students the flow of IC Design, from front-end design to tape-out	
- Assist students to design their own chips and send designs to United Microelectronics Corporation (UMC) for tape-out	
Hardware Design Engineer (Internship), MediaTek	Jun. 2016 – Aug. 2016
- Implement a part of sphere decoding algorithm in Verilog for FPGA	

PROJECTS AND AWARDS

Design Complete Award in IC Design Contest	Mar. 2018
Sponsored by Ministry of Education (MOE) in Taiwan and Taiwan IC Design Society (TICD)	
- Figure out fast enough method to solve computing problem on hardware	
- Implement our method with Verilog in limited time	
Silver Award in MorSensor Contest	Nov. 2017
Held by National Applied Research Lab. in Taiwan	
- Design real-time method for accurate object tracking with inertial measurement unit (IMU)	
- Use Java to develop an application on Android phone	

PUBLICATIONS

<i>Energy-Efficient Accelerator Architecture for Neural Network Training and Its Circuit Design</i>	Jun. 2018
Master's thesis	
Graduate Institute of Electronics Engineering, National Taiwan University, Taiwan	
- Design an architecture with high data utilization to reduce energy cost for neural network accelerator	
- Implement the system based on the process from Taiwan Semiconductor Manufacturing Company (TSMC)	
<i>AOMO: An AI-aided Optimizer for Microservices Orchestration</i> , SIGCOMM 2019 Posters and Demo	Aug. 2019
Xue Leng, Tzung-Han Juang , Yan Chen, Han Liu	
<i>Collision-free Navigation of Human-centered Robots via Markov Games</i> , ICRA 2020	May. 2020
Guo Ye, Qinjie Lin, Tzung-Han Juang , Han Liu	

SKILLS

Programming
Python, C++, Kubernetes, Verilog, CUDA, Java, MATLAB