TZUNG-HAN JUANG

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Area of Interest: Hardware Design, Compilers, High-Level Synthesis, Machine Learning

Programming Skills: Scala, Python, VHDL, Verilog, Assembly, C++, Java

EDUCATION

McGill University, Canada — *2021/01 - Current*
PhD Candidate, Department of Electrical and Computer Engineering — GPA: 4.0/4.0

Northwestern University, USA — *2018/09 - 2020/06*
Master's Degree, Department of Computer Science — GPA: 3.9/4.0

National Taiwan University, Taiwan — *2016/09 - 2018/06*
Master's Degree, Graduate Institute of Electronics Engineering — GPA: 3.9/4.0

National Cheng Kung University, Taiwan — *2013/09 - 2016/06*
Bachelor's Degree, Department of Electrical Engineering — GPA: 3.9/4.0

EXPERIENCE

System Administrator for research group, McGill University — *2022/04 - Current*
- Managing the computing infrastructure for high-level synthesis of neural network accelerators.
- Managing git version control of a bitbucket repository.

Summer Intern Advisor, McGill University — *2022/06 - 2023/10*
- Technical supervision of summer intern (from the University of Electronic Science and Technology of China) to generate Capsule Networks with high-level synthesis.
- Technical supervision of summer intern (from the Indian Institute of Technology) to generate FFT-based convolutions with high-level synthesis.

Research Assistant, Northwestern University — *2019/06 - 2020/12*
- Built a simulation framework for modeling Intel's IC packaging supply chain based on SimPy.
- Designed multi-agent reinforcement learning methods to solve scheduling problems for the supply chain.

Data Science Intern, Intel — *2020/06 - 2020/09*
- Optimized an existing solver (in Python) for managing a supply chain and reduced the run time by 80%.
- Built gradient boosting models for predicting the behaviors of the supply chain.

Hardware Engineering Intern, MediaTek — *2016/06 - 2016/08*
- Implemented a part of Sphere Decoder for 5G communication (in Verilog) and optimized its area usage.

TEACHING

Computer Organization, Tutor, McGill University — *2023/09 - 2023/12*
- Holding tutorials about bus protocols, interrupts, and caches of a computer system.

Compiler Design, Tutor, McGill University — *2023/01 - 2023/04*
- Designed students' projects of code generation and register allocation.

Computer Organization, Tutor, McGill University — *2022/09 - 2022/12*
- Held tutorials about ARM Assembly and lab sessions for display and keyboard control on the DE1-SoC simulator.

Integrated Circuit Design Lab, Tutor, National Taiwan University *2018/01 - 2018/06*
• Assisted students in completing their hardware design projects, which involved Verilog coding, logic synthesis, place and route, as well as IC tape-out flow.
• Guided students to handle the UMC18 process from United Microelectronics Corporation.

Integrated Circuit Design, Grader, National Taiwan University *2017/09 - 2018/01*

Integrated Circuit Design Lab, Tutor, National Taiwan University *2017/02 - 2017/06*

ACADEMIC SERVICE

Registration Chair, ACM International Symposium on Code Generation and Optimization *2022/10 - 2023/03*
• Managed the registration website and resolved registration-related issues of the conference (CGO'23).

AWARDS AND SCHOLARSHIPS

McGill Engineering Doctoral Awards, McGill University *2021/01 - 2023/12*
• This award supports high-caliber engineering Ph.D. students for their tuition and daily expense.

MSc Scholarship, Northwestern University *2019/09 - 2020/06*
• Research assistantship at Northwestern University.

Design Complete Award for Integrated Circuit Design Contest, Taiwan *2018/03*
(Host: National Sun Yat-Sen University, Taiwan)
• A nationwide contest for Verilog hardware description language coding.
• The topic of that year is Huffman coding and RF Indoor Localization Engine.

Silver Award for MorSensor Contest, Taiwan *2017/11*
(Host: National Applied Research Laboratories, Taiwan)
• Led a group for implementing a real-time object-tracking application on Android.
• The Android application was connected to an external Inertial measurement unit (IMU) sensor and detected its location in real time.

PRESENTATIONS

Let Coarse-Grained Resources Be Shared: Mapping Entire Neural Networks on FPGAs
Tzung-Han Juang, Christof Schlaak, and Christophe Dubach
International Conference on Compilers, Architectures, and Synthesis for Embedded Systems 2023 (CASES'23)

Automatic Shareable Function Detection for Hardware Accelerator Synthesis with Functional IRs
Tzung-Han Juang, Christof Schlaak, and Christophe Dubach
ACM Student Research Competition at IEEE/ACM International Symposium on Code Generation and Optimization, Montreal, Canada, Feb 2023

Coarse-Grained Resource Sharing for Entire Neural Networks
Tzung-Han Juang, Christof Schlaak, and Christophe Dubach
1st Languages, Architectures, and Tools for Heterogeneous Computing Workshop, Montreal, Canada, Feb 2023

Data Reshaping and Function Reusing for High-Level Synthesis with Functional IR
Tzung-Han Juang, Christof Schlaak, and Christophe Dubach
9th Compiler-Driven Performance Workshop, Toronto, Canada, Nov 2022

Design Space Exploration of Function Reusing in Functional IRs for Accelerator Generations
Tzung-Han Juang and Christophe Dubach
50th School Of Computer Science Anniversary Poster Session, McGill University, Oct 2022

PUBLICATIONS

Let Coarse-Grained Resources Be Shared: Mapping Entire Neural Networks on FPGAs
Tzung-Han Juang, Christof Schlaak, and Christophe Dubach
(Best Paper Candidate) *ACM Transactions on Embedded Computing Systems (TECS), vol. 22, 5s, no. 114, 2023, presented at the International Conference on Compilers, Architectures, and Synthesis for Embedded Systems 2023 (CASES'23)*
• Designed coarse-grained resource-sharing mechanisms to handle sparse resources such as DSPs on FPGAs.
• Accelerated convolutional neural networks on Intel Arria 10 FPGA and produced competitive performance.
• Optimized accelerators with the consideration of data transfer between the host and FPGA via PCI-Express.
• Contributed to most parts of paper writing.

Optimizing Data Reshaping Operations in Functional IRs for High-level Synthesis
Christof Schlaak, Tzung-Han Juang, and Christophe Dubach
In Proceedings of the 23rd ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES) 2022, page 61–72, New York, NY, USA, 2022
• Designed compiler passes with rewrite rules for optimizing generated hardware architecture.
• Dealt with shifting window and transposition of high-dimensional data, which can have a costly hardware architecture impact on performance and resource usage.
• Evaluated our approaches with convolutional layers on Intel Arria 10 FPGA.

Memory-aware Functional IR for Higher-level Synthesis of Accelerators
Christof Schlaak, Tzung-Han Juang, and Christophe Dubach
ACM Transactions on Architecture and Code Optimization (TACO), vol. 19, no. 2, Jan 2022
• Contributed to the development of VHDL templates for the proposed high-level synthesis framework.
• Managed data transfer between real FPGA and a host computer with PCI-Express.
• Expressed and developed optimizations for convolution layers offering competitive performance with hand-written OpenCL accelerators on Intel Arria 10 FPGA.